问题被转化为标准的混合整数线性规划(mixed integer linear programming,简称 MILP),并通过求解 MILP 问题可以找到能耗优化问题的最优解.

7 总结与展望

随着计算机系统与物理世界的结合越来越紧密,实时系统需要承担的运算任务越来越复杂.为了满足实时系统对高性能的需求,如何在多核硬件上高效集成和部署实时系统是目前学术界和工业界的一个热点问题.本文对现有的面向实时多核嵌入式系统的研究工作进行了综述,介绍了实时多核嵌入式系统的关键设计挑战,并从多核共享资源干扰及管理、多核实时调度、实时程序并行化、多核能耗管理等方面综述了近年来的研究进展,并展望了实时多核系统领域进一步的研究方向.期望本文的介绍能够为相关领域的同行学者提供一定参考.近 10 年来,面向实时多核系统的研究已经取得了一定的成果,但仍存在一些问题需要进一步研究和完善,具体总结如下.

- 资源访问分析技术的融合问题:针对多核共享资源管理和分析技术,现有工作的另一个根本问题是,每种技术通常只考虑一种硬件资源的分析,不同的技术之间通常不存在接口,它们难以被整合在一起以分析整个存储体系结构,也难以综合考虑不同存储层次之间的相互关联.例如,考虑两个共享资源的并行程序,如果一个程序分配较多的缓存资源,从而具有较多的缓存命中,那么这个程序对下一级共享总线的访问将会减少;对于另外一个程序而言,它在共享总线上获得的实际带宽将增加.如果不考虑这些关联,对每一层次的独立分析都不得不考虑最坏情况,那么最后综合得到的分析结果将可能非常悲观(分析值远大于程序客观上的最坏情况执行时间).因此,需要研究不同资源访问分析技术的融合,提高时间分析的准确性和安全性,最终将在实时调度中对各种共享资源的隔离和管理统一起来.这一方向的研究除了理论意义之外,还具有很大的应用价值.
- 功耗模型精度问题:在多核系统的功耗管理研究方面,还需要研究更精准的能耗模型,并需要考虑实时任务多方面的特性对功耗以及执行时间的影响.在目前的研究中,实时任务的功耗和执行时间还只与芯片的频率有关,远不够精确,还需研究更准确的模型以确保能耗计算和时间计算的准确性以及基于相应模型的优化效果.
- 任务抢占切换开销问题:目前,多核调度算法大部分还没有考虑任务之间抢占和任务迁移的开销问题.大部分研究工作都假设任务之间抢占和任务迁移的开销忽略不计或者已经计算入最差执行时间.然而,文献[136]已经发现,任务之间的抢占以及任务在处理器之间的迁移造成的开销是不可忽略的,会导致现在按照 WCET 进行的调度缺少可预测性.如何建立有效的任务抢占切换开销评价体系与方法,并将其无缝集成到当前调度算法中,还需要进一步加以研究和探讨.
- 异构多核调度问题:本文所综述的实时调度问题大多数考虑的是对等多核处理器模型思想,即各个处理器核心具有完全相同的处理能力.然而,现在多核处理器系统的一个重要的发展方向是采用异构处理器架构,其中一个重要的理论问题是如何将“Liu & Layland”资源利用率推广到异构多核处理器.

References:

[1] Turley J. The Essential Guide to Semiconductors. 4th ed., Englewood: Prentice Hall, 2002.

[2] Kopetz H. Real-Time Systems: Design Principles for Distributed Embedded Applications. 2nd ed., Springer-Verlag, 2011.

[3] Salloum CE, Elshuber M, Hoftberger O, Isakovic H, Wasicek A. The ACROSS MPSoC—A new generation of multi-core processors designed for safety-critical embedded systems. Microprocessors & Microsystems, 2013,37(8):1020–1032.

[4] Fisher S. Certifying applications in a multi-core environment: The World’s first multi-core certification to SIL 4. White Paper, SYSGO AG, 2014.

[5] http://www.upcrc.illinois.edu/

[6] http://parlab.eecs.berkeley.edu/

[7] http://www.it.uu.se/research/upmarc

[8] http://www.multipartes.eu/

[9] http://www.across-project.eu/

[10] http://www.certainty-project.eu/

[11] http://www.proxima-project.eu/

[12] Blake G, Dreslinski RG, Mudge T. A survey of multicore processors. IEEE Signal Processing Magazine, 2009,26(6):26–37.

[13] Shi W, Zhang M, Guo YF, Gong R. Technologies of real-time processor architecture: A survey. Computer Engineering and Science, 2015,37(5):857–864 (in Chinese with English abstract).

[14] https://www.nxp.com/docs/en/data-sheet/MPC5643L.pdf

[15] Parkinson PJ. Applying MILS to multicore avionics systems. In: Proc. of the Int'l Workshop on Mils: Architecture and Assurance for Secure Systems (HIPEAC). Stockholm: IEEE, 2016.

[16] Dutta S. Impact of spintronics transducers on the performance of spin wave logic circuit. In: Proc. of the 16th IEEE Int'l Conf. on Nanotechnology (IEEE-NANO). Sendai: IEEE, 2016. 990–993.

[17] Mahapatra R, Lee J, Gupta N, Manners R. Microprocessor evaluations for safety-critical, real-time applications: Authority for expenditure. Technical Report, No.43, DOT/FAA/AR-11/5, US Federal Aviation Administration, 2011.

[18] Kim H, Kandhalu A, Rajkumar R. A coordinated approach for practical OS-level cache management in multi-core real-time systems. Real-Time Systems, 2013,8114:80–89.

[19] Yan J, Zhang W. WCET analysis for multi-core processors with shared L2 instruction caches. In: Proc. of the 2008 IEEE Real-Time and Embedded Technology and Applications Symp. Missouri: IEEE, 2008. 80–89.

[20] Li Y, Suhendra V, Liang Y, Mitra T, Roychoudhury A. Timing analysis of concurrent programs running on shared cache multi-cores. In: Proc. of the IEEE Real-Time Systems Symp. Washington: IEEE, 2009. 56–57.

[21] Calandrino JM, Anderson JH. Cache-Aware real-time scheduling on multicore platforms: Heuristics and a case study. In: Proc. of the 25th Euromicro Conf. on Real-Time Systems (ECRTS). Prague: IEEE, 2008. 299–308.

[22] Cho S, Jin L, Lee K. Achieving predictable performance with on-chip shared l2 caches for many core-based real-time systems. In: Proc. of the 13th IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications. IEEE, 2007. 3–11.

[23] Zhang X, Dwarkadas S, Shen K. Towards practical page coloring-based multicore cache management. In: Proc. of the 4th ACM European Conf. on Computer Systems. Nuremberg: ACM, 2009. 89–102.

[24] Ward BC, Herman JL, Kenna CJ, Anderson JH. Making shared caches more predictable on multicore platforms. In: Proc. of the 25th Euromicro Conf. on Real-Time Systems (ECRTS). Paris: IEEE, 2013. 157–167.

[25] Kim H, Kandhalu A, Rajkumar R. A coordinated approach for practical OS-level cache management in multi-core real-time systems. In: Proc. of the 25th Euromicro Conf. on Real-Time Systems. Paris: DSLP, 2013. 80–89.

[26] Suzuki N, Hyoseung Kim, de Niz D, Andersson B, Wrage L, Klein M, Rajkumar R. Coordinated bank and cache coloring for temporal protectionof memory accesses. In: Proc. of the 16th IEEE Int'l Conf. on Computational Science and Engineering (ICESS). Melbourne, 2013. 685–692.

[27] Lin J, Lu QD, Ding XN, Zhang Z, Zhang XD, Sadayappan P. Gaining insights into multicore cache partitioning: Bridgingthe gap between simulation and real systems. In: Proc. of the 14th IEEE Int'l Symp. on High Performance Computer Architecture (HPCA). Salt Lake City: IEEE, 2008. 367–378.

[28] Chen G, Huang K, Cheng L, Hu B, Knoll A. Dynamic partitioned cache memory for real-time MPSoCs with mixed criticality. Journal of Circuits, Systems and Computers, 2016,25(6):1650062.

[29] Chen G, Hu B, Huang K, Knoll A, Liu D, Stefanov T, Li F. Reconfigurable cache for real-time MPSOCs: Scheduling and implementation. In: Microprocessors and Microsystems. 2016. 200–214.

[30] Chen G. Automatic cache partitioning and time-triggered scheduling for real-time MPSoCs. In: Proc. of the 2014 Int'l Conf. on ReConFigurable Computing and FPGAs (ReConFig14). Cancun: IEEE, 2014. 1–8.

[31] Guan N, Stigge M, Yi W. Cache-Aware scheduling and analysis for multicores. In: Proc. of the Embedded Software, Grenoble. ACM, 2009. 245–254.

[32] Liu TT, Zhao YC, Li MM, Xue CJ. Joint task assignment and cache partitioning with cache locking for WCET minimization on MPSoC. Journal of Parallel and Distributed Computing, 2011,71(11):1473–1483.

[33] Hardy D, Piquet T, Puaut I. Using bypass to tighten WCET estimates for multi-core processors with shared instruction caches. In: Proc. of the 30th IEEE Real-Time Systems Symp. Washington: IEEE, 2009. 68–77.

[34] Chattopadhyay S, Roychoudhury A, Mitra T. Modeling shared cache and bus in multicores for timing analysis. In: Proc. of the 13th Int'l Workshop on Software Compilers for Embedded Systems. Scottsdale: ACM, 2010.

[35] Schranzhofer A, Chen J, Thiele L. Timing analysis for TDMA arbitration in resource sharing systems. In: Proc. of the 16th IEEE Real-Time and Embedded Technology and Applications Symp. San Diego: IEEE, 2010. 215–224.

[36] Kelter T, Falk H, Marwedel P, Chattopadhyay S, Roychoudhury A. Bus-Aware multicore WCET analysis through TDMA offset bounds. Real-Time Systems, 2011,6794(29):3–12.

[37] Rosen J, Andrei A, Eles P, Peng Z. Bus access optimization for predictable implementation of real-time applications on multiprocessor systems-on-chip. In: Proc. of the 28th IEEE Int'l Real-Time Systems Symp. Tucson: IEEE, 2007. 48–60.

[38] Pellizzoni R, Schranzhofer A, Chen J, Caccamo M, Thiele L. Worst case delay analysis for memory interference in multicore systems. In: Proc. of the Design, Automation, and Test in Europe (DATE). Dresden: IEEE, 2010,170(1):741–746.

[39] Gustavsson A, Ermedahl A, Lisper B, Pettersson P. Towards WCET analysis of multicore architectures using UPPAAL. In: Proc. of the Int'l Workshop on Worst-Case Execution Time Analysis. Brussels, 2010. 101–112.

[40] Lü M, Wang Y, Guan N, Yu G. Combining abstract interpretation with model checking for timing analysis of multicore software. In: Proc. of the 31st IEEE Real-Time Systems Symp. San Diego: IEEE, 2010. 339–349.

[41] Yun H, Yao G, Pellizzoni R, Caccamo M, Sha L. Memory access control in multiprocessor for real-time systems with mixed criticality. In: Proc. of the 24th Euromicro Conf. on Real-Time Systems (ECRTS). Pisa: IEEE, 2012. 299–308.

[42] Paolieri M, Quiñones E, Cazorla FJ. Timing effects of DDR memory systems in hard real-time multicore architectures: Issues and solutions. ACM Trans. Embedded Computing System, 2013.

[43] Pao M. An analyzable memory controller for hard real-time CMPs. IEEE Embedded Systems Letters, 2010,1(4):86–90.

[44] Akesson B, Goossens K. Architectures and modeling of predictable memory controllers for improved system integration. In: Proc. of the 2011 Design, Automation Test in Europe Conf. Exhibition (DATE). Grenoble: IEEE, 2011. 1–6.

[45] Liu C, Layland J. Scheduling algorithms for multiprogramming in a hard-real-time environment. Journal of the ACM, 1973.

[46] Davis PI, Burns A. A survey of hard real-time scheduling for multiprocessor systems. ACM Computer Surveys, 2011,43(4):1–44.

[47] Li RF, Liu Y, Xu C. A survey of task scheduling research progress on multiprocessor system-on-chip. Journal of Computer Research And Development, 2008,45(9):1620–1629 (in Chinese with English abstract).

[48] Cousot P, Cousot R. Abstract interpretation: A unified lattice model for static analysis of programs by construction or approximation of fix points. In: Proc. of the POPL. 1977. 238–252.

[49] Li YTS, Malik S. Performance analysis of embedded software using implicit path enumeration. In: Proc. of the 32nd Annual ACM/IEEE Design Automation Conf. (DAC). Brighton: IEEE, 1995. 450–460.

[50] Lü MS, Guan N, Wang Y. Survey of cache analysis for worst-case execution time estimation. Ruan Jian Xue Bao/Journal of Software, 2014,25(2):179–199 (in Chinese with English abstract). http://www.jos.org.cn/1000-9825/4529.htm [doi: 10.13328/j.cnki.jos.004529]

[51] Ungerer T, Cazorla F, Sainrat P, *et al*. Merasa: Multicore execution of hard real-time applications supporting analyzability. IEEE Micro, 2010,30(5):66–75.

[52] Kim H, de Niz D, Andersson B, Klein M, Mutlu O, Rajkumar R. Bounding and reducing memory interference in COTS-based multi-core systems. Real-Time System, 2016,52(3):356–395.

[53] Waez MTB, Dingel J, Rudie K. A survey of timed automata for the development of real-time systems. Computer Science Review, 2013,9:1–26.

[54] Baruah SK, Mok AK, Rosier LE. Preemptively scheduling hard-real-time sporadic tasks on one processor. In: Proc. of the Real-Time Systems Symp. IEEE, 1990. 182–190.

[55] Baruah S, Chen D, Gorinsky S, Mok A. Generalized multiframe tasks. Real-Time Systems, 1999,17(1):5–22.

[56] Stigge M, Ekberg P, Guan N, Wang Y. The digraph real-time task model. In: Proc. of the 17th IEEE Real-Time and Embedded Technology and Applications Symp. Chicago: IEEE, 2011. 71–80.

[57] Stigge M, Ekberg P, Wang Y. The fork-join real-time task model. ACM SIGBED Review, 2013, 20.

[58] Baruah S. The non-cyclic recurring real-time task model. In: Proc. of the 31st IEEE Real-Time Systems Symp (RTSS). San Diego: IEEE, 2010. 173–182.

[59] Saifullah A, Agrawal K, Lu CY, Gill CD. Multi-Core real-time scheduling for generalized parallel task models. In: Proc. of the 31st IEEE Real-Time Systems Symp. (RTSS). San Diego: IEEE, 2010. 217–226.

[60] Chakraborty S, Künzli S, Thiele L. A general framework for analysing system properties in platform-based embedded system designs. In: Proc. of the Design, Automation and Test in Europe (DATE). Munich: IEEE, 2003. 10190.

[61] Cruz R. A calculus for network delay, parts I and II. IEEE Trans. on Information Theory, 1991,37:114–141.

[62] Wandeler E, Thiele L. Characterizing workload correlations in multi processor hard real-time systems. In: Proc. of the IEEE Real-Time and Embedded Technology and Applications Symp. San Francisco: IEEE, 2005. 46–55.

[63] Stoimenov N, Chakraborty S, Thiele L. Interface-Based design of real-time systems. In: Advances in Real-Time Systems. 2012. 83–101.

[64] Chen G, Huang K, Buckl C, Knoll A. Applying pay-burst-only-once principle for periodic power management in hard real-time pipelined multiprocessor systems. ACM Trans. on Design Automation of Electronic Systems (TODAES), 2015,20(2):1–27.

[65] Cheng L, Huang K, Chen G, Hu B, Knoll A. Minimizing peak temperature for pipelined hard real-time systems. In: Proc. of the Design, Automation and Test in Europe, EDA Consortium. 2016. 1090–1095.

[66] Huang K, Thiele L. Performance analysis of multimedia applications using correlated streams. In: Proc. of the EDA Consortium. 2007. 912–917.

[67] Jonsson B, Perathoner S, Thiele L, Wang Y. Cyclic dependencies in modular performance analysis. In: Proc. of the 14th Int'l Conf. on Embedded Software (EMSOFT). Atlanta: ACM, 2008. 179–188.

[68] Carpenter J, Funk S, Holman P, Srinivasan A, Anderson J, Baruah S. A categorization of real-time multiprocessor scheduling problems and algorithms. In: Handbook of Scheduling Algorithms Methods & Models and Performance Analysis, Production Planning & Control. 2004.

[69] Liu C. Scheduling algorithms for multiprocessors in a hard real-time environment. In: Proc. of the Int'l Conf. on Information, Communications and Signal Processing. 1969. 1470–1474.

[70] Burchard A, Liebeherr J. New strategies for assigning real-time tasks to multiprocessor systems. IEEE Trans. on Computers, 1995, 44(12):1429–1442.

[71] Oh Y, Sang HS. Allocating fixed-priority periodic tasks on multiprocessor systems. Real-Time Systems, 1995,9(3):207–239.

[72] Andersson B, Jonsson J. The utilization bounds of partitioned and pfair static-priority scheduling on multiprocessors are 50%. In: Proc. of the IEEE Euromicro Conf. on Real-Time Systems (ECRTS). Porto: IEEE, 2003.

[73] Andersson B, Bletsas K. Sporadic multiprocessor scheduling with few preemptions. In: Proc. of the 2008 Euromicro Conf. on Real-Time Systems (ECRTS). Prague: IEEE, 2008. 322–334.

[74] Kato S, Yamasaki N. Semi-Partitioned fixed-priority scheduling on multiprocessors. In: Proc. of the IEEE Symp. on Real-Time and Embedded Technology and Applications. IEEE Computer Society, 2009. 23–32.

[75] Kato S, Yamasaki N. Portioned static-priority scheduling on multiprocessors. In: Proc. of the IEEE Int'l Symp. on Parallel and Distributed Processing. Sydney: IEEE, 2008. 1–12.

[76] Lakshmanan K, Rajkumar R, Lehoczky JP. Partitioned fixed-priority preemptive scheduling for multi-core processors. In: Proc. of the 2008 Euromicro Conf. on Real-Time Systems (ECRTS). Dublin: IEEE, 2009. 239–248.

[77] Guan N, Stigge M, Wang Y, Yu G. Fixed-Priority multiprocessor scheduling with Liu and Layland's utilization bound. In: Proc. of the IEEE Real-Time and Embedded Technology and Applications Symp. (RTAS). Stockholm: IEEE, 2010. 165–174.

[78] Phillips C, Stein C, Torng E, Wein J. Optimal time-critical scheduling via resource augmentation. In: Proc. of the ACM Symp. on theory of Computing, 2002,32(2):163–200.

[79] Baker T. An analysis of EDF schedulability on a multiprocessor. IEEE Trans. on Parallel Distribution System, 2005,16(8):760–768.

[80] Baker T. An analysis of fixed-priority schedulability on a multiprocessor. Real-Time Systems, 2006,32(1-2):49–71.

[81] Bertogna M, Cirinei M, Lipari G. Improved schedulability analysis of EDF on multiprocessor platforms. In: Proc. of the 17th Euromicro Conf. on Real-Time Systems (ECTRS). Palma de Mallorca: IEEE, 2005. 209–218.

[82] Bertogna M, Cirinei M. Response-Time analysis for globally scheduled symmetric multiprocessor platforms. In: Proc. of the 30th IEEE Int'l Real-Time Systems Symp. (RTSS). Washington: IEEE, 2007. 149–160.

[83] Bertogna M, Baruah S. Tests for global EDF schedulability analysis. Journal of Systems Architecture, 2011,57(5):487–497.

[84] Guan N, Stigge M, Wang Y, Yu G. New response time bounds for fixed priority multiprocessor scheduling. In: Proc. of the 30th IEEE Real-Time Systems Symp. (RTSS). Washington: IEEE, 2009. 387–397.

[85] Sun YC, Lipari G, Guan N, Wang Y. Improving the response time analysis of global fixed-priority multiprocessor scheduling. In: Proc. of the 20th IEEE Conf. on Embedded and Real-Time Computing Systems and Applications. Chongqing: IEEE, 2014. 1–9.

[86] Baruah SK, Cohen NK, Plaxton CG, Varel DA. Proportionate progress: A notion of fairness in resource allocation. Algorithmica, 1996,15(6):600–625.

[87] Baruah SK, Gehrke J, Plaxton CG. Fast scheduling of periodic tasks on multiple resources. In: Proc. of the Int'l Parallel Processing Symp. IEEE, 1995. 280–288.

[88] Anderson JH, Srinivasan A. Mixed pfair/erfair scheduling of asynchronous periodic tasks. In: Proc. of the 13th Euromicro Conf. on Real-Time Systems (ECRTS). Delft: IEEE, 2001. 76–85.

[89] Leontyev H, Chakraborty S, Anderson JH. Multiprocessor extensions to real-time calculus. Real-Time Systems, 2011,47(6): 562–617.

[90] Schranzhofer A, Pellizzoni R, Chen JJ, Thiele L, Caccamo M. Timing analysis for resource access interference on adaptive resource arbiters. In: Proc. of the IEEE Real-Time and Embedded Technology and Applications Symp (RTAS). Chicago: IEEE, 2011. 213–222.

[91] Vestal S. Preemptive scheduling of multi-criticality systems with varying degrees of execution time assurance. In: Proc. of the 30th IEEE Int'l Real-Time Systems Symp. (RTSS). Washington: IEEE, 2007. 239–243.

[92] Burns A, Davis R. Mixed criticality systems—A review. Technical Report, New York: University of York, Department of Computer Science, 2016.

[93] Ren JK, Phan LTX. Mixed-Criticality scheduling on multiprocessors using task grouping. In: Proc. of the 27th Euromicro Conf. on Real-Time Systems (ECRTS). Lund: IEEE, 2015. 25–34.

[94] Chen G, Guan N, Liu D, He Q, Huang K, Stefanov T, Wang Y. Utilization-Based scheduling of flexible mixed-criticality real-time tasks. IEEE Trans. on Computers, 2017,99:1.

[95] Shin I, Easwaran A, Lee I, Hierarchical scheduling framework for virtual clustering of multiprocessors. In: Proc. of the Euromicro Conf. on Real-Time Systems (ECRTS). Prague: IEEE, 2008. 181–190.

[96] Shin I, Lee I. Periodic resource model for compositional real-time guarantees. In: Proc. of the 24th IEEE Real-Time Systems Symp. (RTSS). Toronto: IEEE, 2003. 2–13.

[97] Burmyakov A, Bini E, Tovar E. Compositional multiprocessor scheduling: The GMPR interface. Real-Time Systems, 2014, 50(3):342–376.

[98] Bini E, Bertogna M, Baruah S. Virtual multiprocessor platforms: Specification and use. In: Proc. of the Real-Time Systems Symp. (RTSS). Washington: IEEE, 2009. 437–446.

[99] Lipari G, Bini E. A framework for hierarchical scheduling on multiprocessors—From application requirements to run-time allocation. In: Proc. of the 31st IEEE Real-Time Systems Symp. (RTSS). San Diego: IEEE, 2010. 249–258.

[100] Xi S, Wilson J, Lu C, Gill C. RT-Xen: Towards real-time hypervisor scheduling in Xen. In: Proc. of the 9th ACM Int'l Conf. on Embedded Software (EMSOFT). IEEE, 2011.

[101] Xi SS, Xu M, Lu CY, Phan LTX, Gill C, Sokolsky O, Lee I. Real-Time multi-core virtual machine scheduling in Xen. In: Proc. of the 14th Int'l Conf. on Embedded Software (EMSOFT). New Delhi: IEEE, 2014. 1–10.

[102] Jing W, Guan N, Wang Y. Performance isolation for real-time systems with Xen hypervisor on multi-cores. In: Proc. of the 20th IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA). 2014. 1–7.

[103] Kim H, Rajkumar R. Real-Time cache management for multi-core virtualization. In: Proc. of the 2016 Int'l Conf. on Embedded Software (EMSOFT). Pittsburgh: ACM, 2016. 1–10.

[104] Xu M, Phan L, Choi HY, Lee I. vCAT: Dynamic cache management using CAT virtualization. In: Proc. of the 2017 IEEE Real-Time and Embedded Technology and Applications Symp. (RTAS). Pittsburgh: IEEE, 2017. 211–221.

[105] Vargas R, Quiñones E, Marongi A. OpenMP and timing predictability: A possible union. In: Proc. of the Design, Automation, and Test in Europe (DATE). Grenoble: IEEE, 2015. 617–620.

[106] Li J, Chen JJ, Agrawal K, Lu CY, Gill C, Saifullah A. Analysis of federated and global scheduling for parallel real-time tasks. In: Proc. of the Euromicro Conf. on Real-Time Systems (ECRTS). Madrid: IEEE, 2014. 85–96.

[107] Li J, Luo Z, Ferry D, Agrawal K, Gill CD, Lu CY. Global EDF scheduling for parallel real-time tasks. Real-Time Systems, 2015, 51(4):395–439.

[108] Saifullah A, Ferry D, Li J, Agrawal K, Lu CY, Gill CD. Parallel real-time scheduling of DAGs. IEEE Trans. on Parallel & Distributed Systems, 2014,25(12):3242–3252.

[109] Lakshmanan K, Kato S, Rajkumar R. Scheduling parallel real-time tasks on multi-core processors. In: Proc. of the 31st IEEE Real-Time Systems Symp. (RTSS). San Diego: IEEE, 2010. 259–268.

[110] Melani A, Bertogna M, Bonifaci V, Marchetti-Spaccamela A, Buttazzo GC. Response-Time analysis of conditional DAG tasks in multiprocessor systems. In: Proc. of the IEEE Euromicro Conf. on Real-Time Systems (ECRTS). Lund: IEEE, 2015. 211–221.

[111] Fonseca JC, Nélis V, Raravi G, Pinho LM. A multi-DAG model for real-time parallel applications with conditional execution. In: Proc. of the 30th Annual ACM Symp. on Applied Computing (SAC). New York: ACM. 2015. 1925–1932.

[112] Baruah S, Bonifaci V, Marchetti-Spaccamela A. The global EDF scheduling of systems of conditional sporadic DAG tasks. In: Proc. of Euromicro Conf. on Real-Time Systems (ECRTS). Lund: IEEE, 2015. 222–231.

[113] Silva F, Lopes E, Aude E, Mendes F, Silveira J, Serdeira H, Martins M, Cirne W. Response time analysis of gang scheduling for real time systems. In: Proc. of the Int'l Symp. on Performance Evaluation of Computer and Telecommunication Systems. 2002.

[114] Goossens J, Berten V. Gang ftp scheduling of periodic and parallel rigid real-time tasks. Computer Science, 2012.

[115] Borkar S. Thousand core chips: A technology perspective. In: Proc. of the 44th Annual Design Automation Conf. (DAC). New York: ACM, 2007. 746–749.

[116] Esmaeilzadeh H, Blem E, Amant R, Sankaralingam K, Burger D. Dark silicon and the end of multicore scaling. In: Proc. of the SIGARCH Computer Architecture News. ACM, 2011. 365–376.

[117] Martin SM, Flautner K, Mudge T, Blaauw D. Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads. In: Proc. of the IEEE/ACM Int'l Conf. on Computer Aided Design (ICCAD). ACM/ IEEE, 2002. 721–725.

[118] Jejurikar R, Pereira C, Gupta R. Leakage aware dynamic voltage scaling for real-time embedded systems. In: Proc. of the 41st Design Automation Conf. (DAC). San Diego: ACM, 2004.

[119] Pagani S, Chen J. Energy efficiency analysis for the single frequency approximation (SFA) scheme. In: Proc. of the 19th IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications. IEEE, 2013. 1–25.

[120] Pouwelse J, Langendoen K, Sips HJ. Application-Directed voltage scaling. IEEE Trans. on VLSI Systems, 2003, 812–826.

[121] Aydin H, Yang Q. Energy-Aware partitioning for multiprocessor real-time systems. In: Proc. of the Int'l Parallel and Distributed Processing Symp. Nice: IEEE, 2003. 9.

[122] Moreno G, de Niz D. An optimal real-time voltage and frequency scaling for uniform multiprocessors. In: Proc. of the 2012 IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications. Seoul: IEEE, 2012. 21–30.

[123] Zhu D, Melhem R, Childers B. Scheduling with dynamic voltage/speed adjustment using slack reclamation in multiprocessor real-time systems. In: Proc. of the IEEE Transactions on Parallel and Distributed Systems. Nice: IEEE, 2003. 686–700.

[124] Xu H, Kong F, Deng Q. Energy minimizing for parallel real-time tasks based on level-packing. In: Proc. of the 2012 IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications. Seoul: IEEE, 2012. 98–103.

[125] Chen JJ, Kuo TW. Multiprocessor energy-efficient scheduling for real-time tasks with different power characteristics. In: Proc. of the 2005 Int'l Conf. on Parallel Processing (ICPP). Oslo: IEEE, 2005. 13–20.

[126] Lu J, Guo Y. Energy-Aware fixed-priority multi-core scheduling for real-time systems. In: Proc. of the 17th IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications. Toyama: IEEE, 2011. 277–281.

[127] Liu J, Guo JH. Energy efficient scheduling of real-time tasks on multi-core processors with voltage islands. In: Future Generation Computer System. 2016. 202–210.

[128] Kong F, Yi W, Deng Q. Energy-Efficient scheduling of real-time tasks on cluster-based multicores. In: Proc. of the 2011 Design, Automation & Test in Europe (DAC). Grenoble: ACM, 2011. 1135–1140.

[129] Guan N, Stigge M, Yi W, Yu G. Fixed-Priority multiprocessor scheduling with Liu and Layland's utilization bound. In: Proc. of the 16th IEEE Real-Time and Embedded Technology and Applications Symp. Stockholm: IEEE, 2010. 165–174.

[130] Lakshmanan K, Rajkumar R, Lehoczky J. Partitioned fixed-priority preemptive scheduling for multi-core processors. In: Proc. of the 21st Euromicro Conf. on Real-Time Systems. Dublin: IEEE, 2009. 239–248.

[131] ITRS 2011. Int'l Technology Roadmap for Semiconductors. 2011. http://www.itrs.net/reports.html

[132] Chen G, Huang K, Buckl C, Knoll A. Energy optimization with worst-case deadline guarantee for pipelined multiprocessor systems. In: Proc. of the Design, Automation and Test in Europe (DATE). Grenoble: ACM, 2013. 45–50.

[133] Chen G, Huang K, Knoll A. Energy optimization for real-time multiprocessor system-on-chip with optimal DVFS and DPM combination. ACM Trans. on Embedded Computing Systems (TECS), 2014,13:40.

[134] Wang Y, Liu H, Liu D, Qin ZW, Shao ZL, Sha E. Overhead-Aware energy optimization for real-time streaming applications on multiprocessor system-on-chip. ACM Trans. on Design Automation of Electronic Systems (TODAES), 2011,16(2):1–32.

[135] Chen G, Huang K, Knoll A. Adaptive dynamic power management for hard real-time pipelined multiprocessor systems. In: Proc. of the 20th IEEE Int'l Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA). Chongqing: IEEE, 2014. 1–10.

[136] Brandenburg BB, Calandrino JM, Anderson JH. On the scalability of real-time scheduling algorithms on multicore platforms: A case study. In: Proc. of the Real-Time Systems Symp. Tennessee: IEEE, 2008. 157–169.

附中文参考文献:

[13] 石伟,张明,郭御风,龚锐.实时微处理器体系结构综述.计算机工程与科学,2015,37(5):857–864.

[47] 李仁发,刘彦,徐成.多处理器片上系统任务调度研究进展评述.计算机研究与发展,2008,45(9):1620–1629.

[50] 吕鸣松,关楠,王义.面向 WCET 估计的 Cache 分析研究综述.软件学报,2014,25(2):179–199. http://www.jos.org.cn/1000-9825/4529.htm [doi: 10.13328/j.cnki.jos.004529]

陈刚(1985－),男,湖北咸宁人,博士,副教授,CCF 会员,主要研究领域为嵌入式系统,实时系统,计算机体系结构.

吕鸣松(1980－),男,博士,副教授,CCF 会员,主要研究领域为实时系统时间分析,实时操作系统.

关楠(1981－),男,博士,教授,CCF 会员,主要研究领域为实时系统,嵌入式系统.

王义(1961－),男,博士,教授,博士生导师,CCF 会员,主要研究领域为形式化方法,实时嵌入式系统.